REMARKS

This Amendment responds to the Office Action dated September 15, 2004 in which the Examiner rejected claim 8 under 35 U.S.C. §112, second paragraph, rejected claims 7-9 under 35 U.S.C. §102(e), objected to claims 10-13 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form and stated that claims 1-6 and 14-17 are allowed.

As indicated above, claim 8 has been amended in order to more particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Applicant respectfully submits that the amendment does not narrow the literal scope of the claim. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claim 8 under 35 U.S.C. §112, second paragraph.

Claim 7 claims a memory device comprising a plurality of memory cells, a read amplifying circuit and a current path forming section. The plurality of memory cells store information by a change in respective electric resistance, and are arranged in one memory cell array. The read amplifying circuit performs parallel data reading from a plurality of selected memory cells selected simultaneously among the plurality of memory cells. The current path forming section forms a plurality of read current paths respectively corresponding to the plurality of selected memory cells between the read amplifying circuit and a supply source of a power supply potential. The plurality of read current paths is separated from each other at least in the memory cell array.

Through the structure of the claimed invention a) having a current path forming section forming read current paths between read amplify circuits and a supply source of a power supply potential and b) having a plurality of read current

paths separated from each other at least in a memory cell array, as claimed in claim 7, the claimed invention provides a memory device in which the influence of electric resistance is reduced when a plurality of data are simultaneously read. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claims 7-9 were rejected under 35 U.S.C. §102(e) as being anticipated by *Muranaka et al.* (U.S. Publication No. 2002/0071308).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which are set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Muranaka et al. appears to disclose [0007] a semiconductor memory device that has achieved a high-reliability large-storage capacity. [0038] The memory array has memory cells MC provided at around the intersections of write word lines WWL, read word lines RWL, and write bit lines WBL, read bit lines RBL perpendicular to those word lines. The write word lines WWL and read word lines RWL are respectively selected by write and read word drivers that are provided on both sides (in FIG. 1, top and bottom sides) of the memory array in the extension direction of those word lines, though not particularly limited thereto. [0098] The data bus 1 has 512 read/write amplifiers #0.about.#511 provided thereon. Each of the read/write amplifiers #0.about.#511 has a D/A (digital/analog) converter and an A/D (analog/digital) converter. [0099] The number of memory arrays is 64, though not particularly limited thereto, and each of the memory arrays constitutes a memory bank. Each memory array has 4096 word lines and 512 bit lines. The word lines and bit lines include the write word lines WWL, read word lines RWL, write bit lines WBL

and read bit lines RBL. [0100] The I/O selection circuits select any one of the 64 memory banks (or memory mats) and connect the 512 pairs of write bit lines and read bit lines of the selected memory bank to the corresponding signal lines of the data bus 2. The write word lines and read word lines of each memory array are selected by a word driver. [0102] The row address and column address are supplied in a time-sharing manner from address terminals A0.about.A11 to an address register. A part of the address signal in this address register is supplied to a mode register, and used as part of the commands. The row-based address signal A0.about.A11 (12 bits) fed in a time-sharing manner is held in a row address latch, and processed by a decoder to form a ({fraction (1/4096)}) selection signal. The column-based address signal A0.about.A5 (6 bits) fed in a time-sharing manner is held in a column address latch, and processed by a decoder to form a ({fraction (1/64)}) selection signal, or a selection signal for selecting any one of the 64 memory banks or memory mats.

Thus, *Muranaka et al.* merely discloses a semiconductor memory device having a number of memory cells arrays (i.e. 64 arrays) and a number of read/write amplifiers (0-511) connected to a data bus. Nothing in *Muranaka et al.* shows, teaches or suggests a) a current path forming section forming a plurality of read current paths between a read amplifying circuit and a supply source of a power supply potential and b) a plurality of read current paths separated from each other at least in the memory cell array as claimed in claim 7. Rather, *Muranaka et al.* merely discloses a number of memory cells arrays and a number of read/write amplifiers which are connected to a data bus.

Since nothing in *Muranaka et al.* shows, teaches or suggests a) a current path forming section forming current paths between a read amplifying circuit and a supply source of power supply potential and b) a plurality of read current paths separated from each other at least in a memory cell array as claimed in claim 7, Applicant respectfully requests the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §102(e).

Claims 8-9 depend from claim 7 and recite additional features. Applicant respectfully submits that claims 8-9 would not have been anticipated by *Muranaka et al.* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 8-9 under 35 U.S.C. §102(e).

Since objected to claims 10-13 depend from allowable claims, Applicant respectfully requests the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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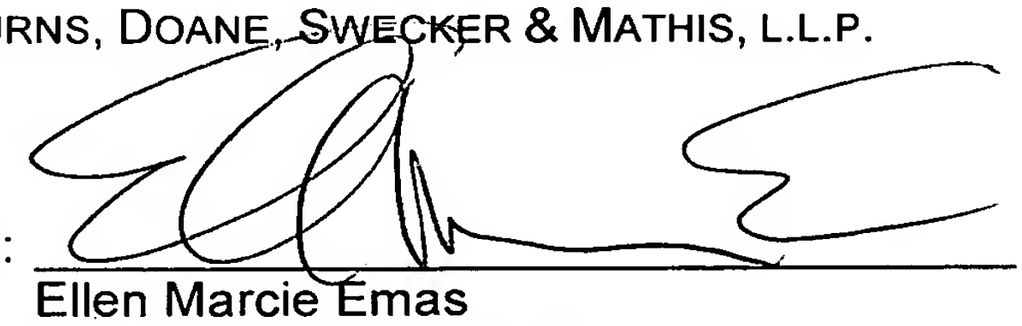
Date: December 13, 2004

By: 

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